than that of a margin part of a second gate electrode constructing the second MOS transistor in the ordinary region. A length of the margin part of the second gate electrode is X. The length of the margin part of the first gate electrode is $X + \propto$ where $0 < \propto \leq X$.

Through the structure of the claimed invention a) having first and second MOS transistors, each having a margin part and b) the length of the margin part of the first gate electrode is larger by $\propto$ than that of the margin part of the second gate electrode and where $0 < \propto \leq X$, as claimed in claim 1, the claimed invention provides a semiconductor device in which an end portion of the first gate electrode completely reaches an upper portion of the insulating film so that the first gate electrode is prevented from partial reduction of the gate length and therefore prevents occurrence of current leakage between source/drain regions which are formed on the exterior of both side surfaces of the first gate electrode. The prior art does not show, teach or suggest first and second MOS transistors each having a margin part where the length of the margin part of the first gate electrode of the first transistor is larger by $\propto$ than the margin part of the second gate electrode of the second transistor and where $0 < \propto \leq X$ as claimed in claim 1.

Claim 12 claims a method of fabricating a semiconductor device on the basis of a layout design, the layout design is achieved by a process comprising the steps of; first, designing a layout of an active area on a plane. The active area is defined from an insulating film by a boundary including a first edge extending along a first direction and a second edge extending along the first direction and a third edge connected between one ends of the first and second edges extending along a second direction different from the first direction. The first to third edges form a step shape so that the second edge is

depressed toward an inside of said active area beyond the first edge. Next, a layout of a first gate electrode of a first MOS transistor on the active area is designed. One end of the first gate electrode extends to an outside of the active area across the first edge in a vertical direction to the first direction. Finally, a layout of a second gate electrode of a second MOS transistor on the active area is designed. One end of the second gate electrode extends to an outside of the active area across the second edge in a vertical direction to the first direction. A length y from the second edge to the one end of the second gate electrode is longer than a length x from the first edge to the one end of the first gate electrode where $y = x + \propto$ where $0 < \propto \leq x$.

Through the method of the claimed invention having a length y from the second edge to the one end of the second gate electrode being longer than a length x from the first edge to the one end of the first gate electrode, where $y = x + \propto$ and where $0 < \propto \leq x$, as claimed in claim 12, the claimed invention provides a method of forming a semiconductor device in which an end portion of the first gate electrode completely reaches an upper portion of the insulating film so that the first gate electrode is prevented from partial reduction of the gate length. The prior art does not show, teach or suggest the method as claimed in claim 12.

Claims 1 and 12 were rejected under 35 U.S.C. § 103 as being anticipated by *Jassowski et al.* (U.S. Patent No. 5,668,389).

Applicants respectfully traverse the Examiner's rejection of the claims under 35 U.S.C. §103. The claims have been reviewed in light of the Office Action, and for

reasons which will be set forth below, it is respectfully requested that the Examiner withdraws the rejection of the claims and allows the claims to issue.

Jassowski et al. appears to disclose providing more available space by which individual cells may be connected to conductors leading to circuitry outside the cell. In Fig. 2 a portion of an exemplary cell 9 is shown. The cell 9 is a typical cell of semiconductor devices which may be positioned on a semiconductor substrate as a portion of a group of cells which provide some larger circuit function. The individual cells 9 in each row are each aligned to utilize these power buses so that the power buses 12 and 14 lie within but near to the boundaries of all of the typical cells 9. Once the cells 9 and all other portions of the larger circuit have been laid out, connections are provided between the individual cells 9 and other circuit elements which are carried on the particular substrate.

Thus, the object of *Jassowski et al.* is to provide more available space to connect individuals cells to conductors. Nothing in *Jassowski et al.* shows, teaches or suggests how to prevent current leakage between source and drain regions by providing the margin part of a gate electrode formed in a depressed region to have a larger length than a gate electrode formed in a ordinary region, where the length of gate electrode in the ordinary region is X, the length of the margin part of a gate electrode in the depressed region is $X+\alpha$ and where $0<\alpha\leq X$ as claimed in claims 1 and 12. Rather, *Jassowski et al.* merely discloses providing more available space for individual cells to be connected to conductors.

Furthermore, Applicant respectfully traverse the Examiner's statement "given that end caps margins of varying lengths are known, it would have been obvious to one of ordinary skill in the art... to form the various end caps such that their respective margins satisfy the stated equation's relationship, the specific length ultimately chosen being dependent only upon conventional and well known consideration". In particular, *Jassowski et al.* is merely directed to providing additional space and is not directed to preventing current leakage. Therefore, even assuming arguendo that the margins of *Jassowski et al.* can be adjusted, they would not be adjusted to prevent current leakage and thus would not fall within the range of $\propto$ as claimed in claims 1 and 12.

Also, *Jassowski et al.* clearly discloses that the margin part 3 formed in the ordinary region has a length greater than the margin part 2 formed in the depressed region (see Fig. 2 attached to previous response of November 9, 2000). However, as claimed in claims 1 and 12, the margin part of the gate electrode formed in the depressed region is longer than the length of the margin part formed in the ordinary region. Thus, *Jassowski et al.* teaches away from the claimed invention since the lengths in *Jassowski et al.* are the opposite of the claimed invention.

Finally, although *Jassowski et al.* discloses a margin 1 in a second depressed region having a length greater than the margin 2 in the first depressed region or the margin 3 in the ordinary region, the length of the margin part 1 is far greater than the other margin parts and thus does not fall within the equation that $0 < \propto \leq X$ as claimed in claims 1 and 12.

Since nothing in *Jassowski et al.* shows, teaches or suggests that the length of the margin part of the gate electrode in the depressed region is larger than the margin part of the gate electrode in the ordinary region and where $0 < \propto \leq X$ as claimed in claims 1 and 12, it is respectfully requested that the Examiner withdraws the rejection to claims 1 and 12 under 35 U.S.C. §103.

Since claim 2 depends from a generic claim it is respectfully requested that the Examiner allow claim 2.

Thus it now appears that the application is in condition for reconsideration and allowance. Reconsideration and allowance at an early date are respectfully requested.

If for any reason the Examiner feels that the application is not now in condition for allowance, it is respectfully requested that the Examiner contact, by telephone, the Applicants' undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this case.

In the event that this paper is not timely filed within the currently set shortened statutory period, Applicants respectfully petition for an appropriate extension of time. The fees for such extension of time may be charged to our Deposit Account No. 02-4800.

In the event that any additional fees are due with this paper, please charge our Deposit Account No. 02-4800.

Respectfully submitted,

BURNS, DOANE, SWECKER & MATHIS, L.L.P.

By: _____
Ellen Marcie Emas
Registration No. 32,131

P.O. Box 1404
Alexandria, Virginia 22313-1404
(703) 836-6620

Date: June 5, 2001